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NEC Electronics Inc.

μPD70616 (V60™) 32-BIT VIRTUAL MEMORY CMOS MICROPROCESSOR

T-49-17-32

PRELIMINARY INFORMATION

Description

The μPD70616 (V60) is a high-performance, second-generation 32-bit microprocessor designed for a wide range of applications including personal computers, engineering workstations, and industrial controllers. The V60 includes advanced features such as thirty-two 32-bit general-purpose registers and a powerful instruction set optimized for high-level languages and operating systems such as UNIX™ and MS-DOS®. The on-chip demand-paged memory management and floating point units further increase performance and design flexibility.

Performance in the μPD70616 is enhanced by pipelining internal operations such as instruction prefetch, instruction decode, address translation, and instruction execution. Software development and debugging is fully supported by instruction breakpoints, single-step traps, and address traps. Emulation mode allows porting of μPD70108/μPD70116 application software to run without modification and with the full protection of the demand-paged virtual memory system. The ability to execute software from the large established base of μPD70108/μPD70116 applications under a host operating system such as UNIX provides an upgrade path from 16-bit architectures yet preserves existing software investments.

Features

- ☐ 32-bit high-performance CMOS microprocessor
- ☐ Thirty-two 32-bit general-purpose registers
- ☐ On-chip demand-paged memory management unit
  - — 4-gigabyte virtual address space
  - — 2-level translation scheme (area/page)
  - — 4 levels of protection
  - — 16-megabyte physical address space
  - — 16 entry translation lookaside buffer (TLB)
- ☐ Supported data types include
  - — 8-, 16-, 32-, 64-bit integers
  - — 32-, 64-bit floating point
  - — 8-, 16-bit characters
  - — Bit, bit field and bit string
- ☐ 21 powerful addressing modes plus bit addressing
- ☐ Context switching and operating system support
- ☐ V20™/V30™ emulation mode
- ☐ Flexible hardware debugging support
  - — Breakpoints
  - — Instruction trace
  - — Address traps
- ☐ Functional redundancy monitor (FRM)

Ordering Information

Part Number	Package	Maximum Frequency
μPD70616R	68-pin PGA	16 MHz

Pin Identification

Symbol	Function
A_{23}-A_0	24-bit address bus output
D_{15}-D_0	16-bit data bus I/O
ST2-ST0	Bus status output
$\overline{MRQ}$	Memory request output
R/$\overline{W}$	Read/write output
$\overline{DS}$	Data strobe output
$\overline{BCY}$	Bus cycle output
DL1-DL0	Data length output
$\overline{FAS}$	First data access output
$\overline{UBE}$	Upper byte enable output
$\overline{READY}$	Ready input
BMODE (FRM)	Bus mode input Functional redundancy monitor
$\overline{BLOCK}$ ($\overline{MSMAT}$)	Bus lock output Mismatch
$\overline{BERR}$	Bus error input
BFREZ	Bus freeze input
RT/$\overline{EP}$	Retry/exception input
NMI	Non-maskable interrupt input
INT	Interrupt input
$\overline{HLDRQ}$	Hold request input
$\overline{HLDAK}$	Hold acknowledge output
$\overline{CPBUSY}$	Coprocessor busy input
RESET	Reset input
CLK	Clock input
V_{DD}	Power
GND	Ground

UNIX is a trademark of AT&T Bell Labs.

MS-DOS is a registered trademark of Microsoft Inc.

V20, V30, and V60 are trademarks of NEC Corporation.

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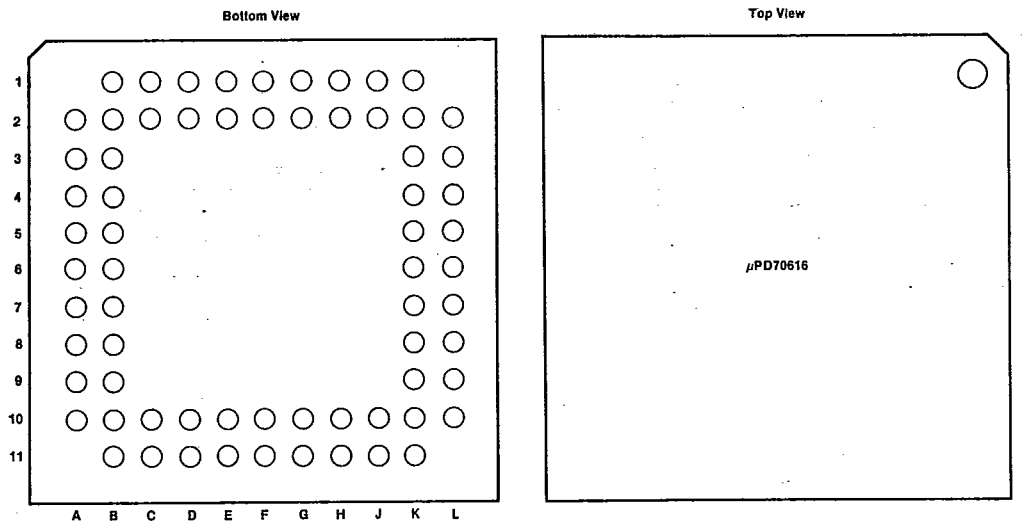
Pin Configuration



Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	D_1	B9	D_{13}	F10	R/$\overline{W}$	K4	A_8
A3	D_3	B10	D_{15}	F11	CLK	K5	A_{10}
A4	D_5	B11	$\overline{HLDRQ}$	G1	ST2	K6	GND
A5	D_7	C1	DL1	G2	V_{DD}	K7	A_{13}
A6	D_9	C2	DL0	G10	V_{DD}	K8	A_{15}
A7	D_{11}	C10	BFREZ	G11	$\overline{MRQ}$	K9	A_{17}
A8	D_{12}	C11	RT/$\overline{EP}$	H1	ST1	K10	A_{20}
A9	D_{14}	D1	INT	H2	ST0	K11	A_{19}
A10	$\overline{HLDAK}$	D2	$\overline{NMI}$	H10	$\overline{UBE}$	L2	A_3
B1	D_0	D10	$\overline{BERR}$, RT/$\overline{EP}$	H11	A_{23}	L3	A_5
B2	RESET	D11	$\overline{READY}$	J1	A_0	L4	A_7
B3	D_2	E1	$\overline{CPBUSY}$	J2	A_1	L5	A_9
B4	D_4	E2	$\overline{FAS}$	J10	A_{22}	L6	A_{11}
B5	D_6	E10	$\overline{BCY}$	J11	A_{21}	L7	A_{12}
B6	D_8	E11	$\overline{DS}$	K1	A_2	L8	A_{14}
B7	D_{10}	F1	$\overline{BLOCK}$	K2	A_4	L9	A_{16}
B8	GND	F2	BMODE	K3	A_6	L10	A_{18}

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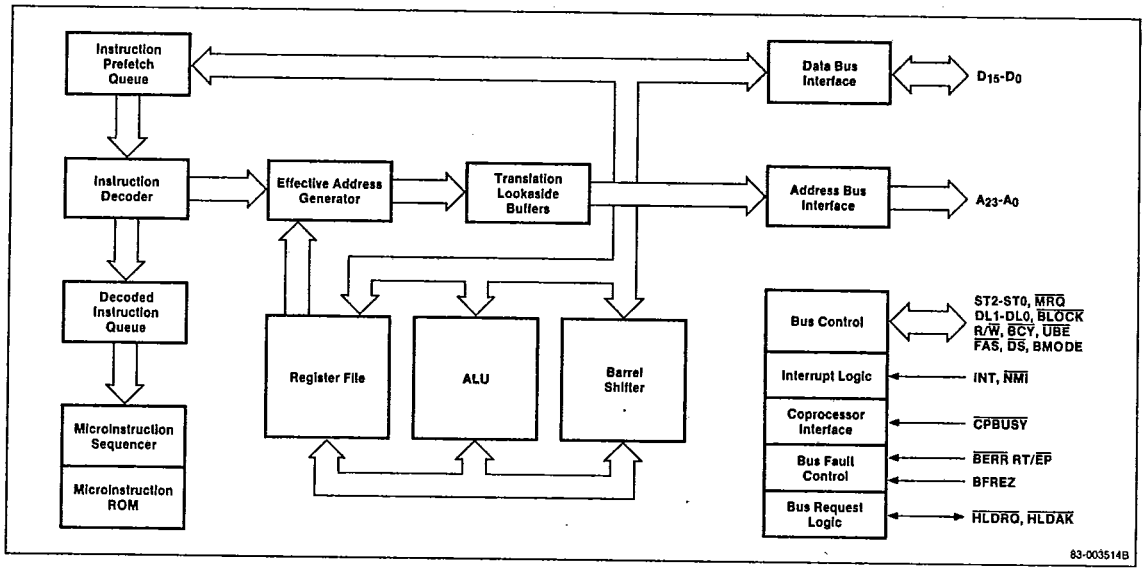
Block Diagram



Applications

V60 CPU Design Example 1